Claims

What is claimed as new and desired to be protected by Letter Patent of the United States is:

1. A digital phase locked loop comprising of :
   A modified phase detector;
   A digital loop filter;
   A numerically controlled oscillator.
2. A modified phase detector as in claim 1, wherein the phase detector produces a numerical output directly proportional to the phase difference between the inputs to the detector.
3. A digital loop filter as in claim 1, comprising of
   A digital integrator having a scalable clock rate;
   An adder wherein one input not connected to the digital integrator is scalable.
4. A numerically controlled oscillator as in claim 1, wherein two digital inputs are available, one to control the center frequency of the oscillator, and the other to change the frequency in accordance with instructions from the loop filter.
5. A digital phase locked loop comprising of:
   A phase digitizer;
   A digital subtractor;
   A digital loop filter;
   A modified numerically controlled oscillator.
6. A phase digitizer as in claim 5, wherein the output of the digitizer in response to an instructing clock pulse, is the instantaneous phase of its input signal at the moment of the instructing clock pulse.
7. A subtractor as in claim 5, wherein the subtractor calculates the difference between the instantaneous phase of the input signal reported by the phase digitizer, and the instantaneous phase of the accumulator in the numerically controlled oscillator at the time of the instructing clock pulse.
8. A digital loop filter as in claim 5, comprising of
   A digital integrator having a scalable clock rate;
   An adder wherein one input not connected to the digital integrator is scalable.
9. A numerically controlled oscillator as in claim 5, wherein two digital inputs are available, one to control the center frequency of the oscillator, and the other to change the frequency in accordance with instructions from the loop filter.
10. A numerically controlled oscillator as in claim 5, further modified to output the instantaneous phase accumulated by the accumulator.
11. A digital phase locked loop comprising of :
    A phase detector;
    A digital counter;
    A numerically controlled oscillator.
12. A phase detector as in claim 11, wherein the phase detector produces digital commands indicating the polarity of a phase error.
13. A digital counter as in claim 11, capable of counting up or counting down.
14. A numerically controlled oscillator as in claim 1, wherein two digital inputs are available, one to control the center frequency of the oscillator, and the other to change the frequency in accordance with instructions from the loop filter.
15. A digital phase locked loop comprising of :
    A phase digitizer;
    A digital magnitude comparator;
    A digital counter;
    A numerically controlled oscillator.
16. A phase digitizer as in claim 15, wherein the output of the digitizer in response to an instructing clock pulse, is the instantaneous phase of its input signal at the moment of the instructing clock pulse.